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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,012	02/11/2004	Richard W. Foote	P05792	3404
23990	7590	09/23/2005	EXAMINER	
DOCKET CLERK P.O. DRAWER 800889 DALLAS, TX 75380			FULK, STEVEN J	
			ART UNIT	PAPER NUMBER
			2891	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/777,012

Applicant(s)

FOOTE ET AL.

Examiner

Steven J. Fulk

Art Unit

2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 22-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/16/04.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-21, in the reply filed on September 6, 2005 is acknowledged. The traversal is on the ground(s) that examination of apparatus claims 2-21 will necessarily require a determination as to whether the prior art teaches simultaneously manufacturing at least one double poly bipolar transistor and at least one double poly MOS transistor, and thus there would be no burden to examine claims 22-42 which describe a method of manufacturing such a device. This is not found persuasive because the process limitations of simultaneous manufacture found in apparatus claims 2-21 invoke the product-by-process doctrine. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps (*MPEP § 2113*). Therefore it will not be required to determine if the process steps are performed simultaneously.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Sachitano et al. '640. Where product-by-process limitations are recited, the claims are limited only by the structure implied by the steps, not the manipulations of the steps. For example, anticipation of claim 2 does not require that the two doping steps be performed simultaneously.

Sachitano et al. discloses a mixed bipolar-CMOS apparatus comprising a double-poly bipolar transistor and a double-poly metal oxide semiconductor (MOS) transistor on a substrate, wherein an extrinsic base of the bipolar transistor and a gate of the MOS transistor are formed of doped polysilicon (col. 8, lines 17-45). The reference discloses the substrate having an implanted region used as an intrinsic base of the bipolar transistor and lightly doped drain of the MOS transistor (col. 8, lines 45-49).

Sachitano et al. also discloses an emitter of the bipolar transistor, a deep collector of the bipolar transistor, and separated source/drain regions of the MOS transistor that are all formed of doped polysilicon (col. 8, lines 42-45; col. 8, line 66 – col. 9, line 6.). The reference discloses a device having NMOS and PMOS transistors (col. 1, lines 11-13; col. 7, lines 13-16), and describes mixed bipolar-CMOS devices that include both NPN or PNP devices (col. 1, lines 63-66).

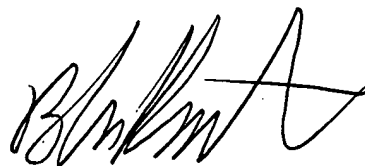
Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - a. Bertotti et al. '142, Chen et al. ' 564, and Johansson et al. '608 disclose double polysilicon bipolar-CMOS devices.
 - b. Gahle '279, Ratnakumar '784, Lechaton et al. '726, and Maeda et al. '751 disclose bipolar-CMOS devices.
5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
9/21/05

A handwritten signature in black ink, appearing to read 'B. William Baumeister', written in a cursive style.

**B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER**